CLAIMS:

What is claimed is:

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1. A circuit comprising:
a plurality of switches coupled to a plurality of registers, the plurality of registers to control the plurality of switches;
wherein the plurality of switches are coupled to a plurality of universal serial bus (USB) ports based on a USB device bandwidth balancing process.

2. The circuit of claim 1, wherein the USB device balancing process balances USB bandwidth load by USB device class.

3. The circuit of claim 2, wherein the USB device class is determined from a USB device descriptor.

4. The circuit of claim 1, wherein the USB device balancing process to balance USB bandwidth load by USB device use information and bandwidth consumption information.

5. The circuit of claim 1, wherein a plurality of USB signals are routed through the plurality of switches to the plurality of USB ports dynamically.

6. A system comprising:
a processor;
a memory coupled to the processor;
a north bridge coupled to a bus and the processor;
a south bridge coupled to the bus; and
a universal serial bus (USB) bandwidth load balancing circuit.

7. The system of claim 6, wherein the USB bandwidth load balancing circuit comprises:
a plurality of switches coupled to a plurality of registers, the plurality of registers to control the plurality of switches, wherein the plurality of switches are coupled to a plurality of universal serial bus (USB) ports based on a USB device bandwidth balancing process.

8. The system of claim 7, wherein the USB device balancing process to balance USB bandwidth load by USB device class.

9. The system of claim 8, wherein the USB device class is determined from a USB device descriptor.

10. The system of claim 7, wherein the USB device balancing process to balance USB bandwidth load by USB device use information and bandwidth consumption information.

11. The system of claim 7, wherein a plurality of USB signals are routed through the plurality of switches to the plurality of USB ports dynamically.

12. The system of claim 1, the south bridge further comprising:
a USB host controller coupled to a plurality of root hubs, the plurality of root hubs coupled to the USB bandwidth load balancing circuit.

13. A method comprising:
determining allocation of a plurality of USB root hubs; and
switching a plurality of USB root hub USB device assignments.

14. The method of claim 13, further comprising:
reading a USB descriptor for a USB device; and
writing a plurality of USB root hub allocation information to a plurality of registers coupled to a USB bandwidth load balancing circuit.

15. The method of claim 14, wherein the USB bandwidth load balancing circuit comprises:
a plurality of switches coupled to the plurality of registers, the plurality of registers to control the plurality of switches, wherein the plurality of switches are coupled to a plurality of USB ports based on a USB device bandwidth balancing process.

16. The method of claim 15, further comprising:
determining an attached USB device's class;
distinguishing USB device classes;
allowing at least two low bandwidth USB class devices to couple to a same USB root hub;

allowing at least one low bandwidth USB class device and at least one high bandwidth USB class device to couple to a same root hub; and

preventing a first high bandwidth USB class device and a second high bandwidth USB class device to couple to a same USB root hub.

17. The method of claim 16, wherein USB device classes are determined from a USB device descriptor.

18. The method of claim 16, wherein switching the plurality of USB root hub USB device assignments is dynamic.

19. The method of claim 15, further comprising monitoring each of an attached USB device's use and USB bandwidth consumption, wherein the USB device balancing process to balance USB bandwidth load by the USB device's use information and bandwidth consumption information.

20. The method of claim 19, wherein switching USB root hub USB device assignments is dynamic.

21. A program storage device readable by a machine comprising instructions that cause the machine to:

determine allocation of a plurality of USB root hubs; and

switching a plurality of USB root hub USB device assignments.

22. The program storage device of claim 21, further comprising instructions that cause the machine to:

read a USB descriptor for a USB device; and

write a plurality of USB root hub allocation information to a plurality of registers coupled to a USB bandwidth load balancing circuit.

23. The program storage device of claim 22, wherein the USB bandwidth load balancing circuit comprises:

a plurality of switches coupled to the plurality of registers, the plurality of registers to control the plurality of switches, wherein the plurality of switches are coupled to a plurality of USB ports based on a USB device bandwidth balancing process.

24. The program storage device of claim 23, further comprising instructions that cause the machine to:

determine an attached USB device's class;

distinguish USB device classes;

allow at least two low bandwidth USB class devices to couple to a same USB root hub;

allow at least one low bandwidth USB class device and at least one high bandwidth USB class device to couple to a same root hub; and

prevent a first high bandwidth USB class device and a second high bandwidth USB class device to couple to a same USB root hub.

25. The program storage device of claim 24, wherein USB device classes are determined from a USB device descriptor.

26. The program storage device of claim 24, wherein switching USB root hub USB device assignments is dynamic.

27. The program storage device of claim 23, further comprising instructions that cause the machine to:

monitor each of an attached USB device's use and USB bandwidth consumption, wherein the USB device balancing process to balance USB bandwidth load by the USB device's use information and bandwidth consumption information.

28. The program storage device of claim 27, wherein switching the plurality of USB root hub USB device assignments is dynamic.